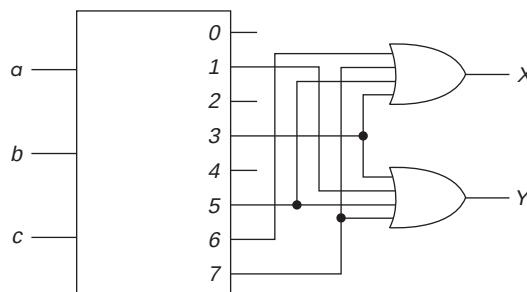


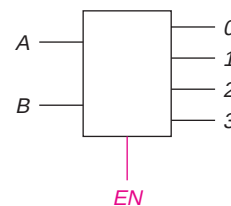
6. We need to determine whether a three-bit number, a_3, a_2, a_1 , is equal to another number, b_3, b_2, b_1 , or if it is greater than that number. (We do not need an output for less than.)
- Show how the 7485 would be connected to accomplish this.
 - Implement this with AND and OR gates.
 - Assuming that the 7485 costs \$1, what must 7400 series AND and OR gate packages cost to make the AND/OR implementation less expensive?
- *7. Consider the following circuit with an active high output decoder. Draw a truth table for X and Y in terms of a , b , and c .



8. We wish to design a decoder, with three inputs, x, y, z , and eight active high outputs, labeled 0, 1, 2, 3, 4, 5, 6, 7. There is no enable input required. (For example, if $xyz = 011$, then output 3 would be 1 and all other outputs would be 0.)

The **only** building block is a two-input, four-output decoder (with an active high enable), the truth table for which is shown below.

<i>EN</i>	<i>A</i>	<i>B</i>	0	1	2	3
0	X	X	0	0	0	0
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1



Draw a block diagram of the system using as many of these building blocks as are needed.

- *9. We want to implement a full adder; we'll call the inputs a, b , and c and the outputs s and c_{out} . As always, the adder is described by the following equations:

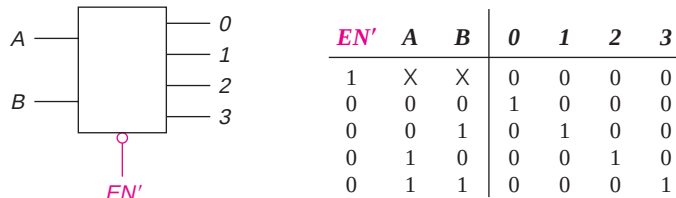
$$s(a, b, c) = \Sigma m(1, 2, 4, 7)$$

$$c_{out}(a, b, c) = \Sigma m(3, 5, 6, 7)$$

To implement this, all we have available are two decoders (as shown below) and two OR gates. Inputs a and b are available both uncomplemented and complemented; c is available only

5.10 Exercises

uncomplemented. Show a block diagram for this system. Be sure to label all of the inputs to the decoders.



10. Show the block diagram for a decoder, the truth table for which is shown below. The available components are one-, two-, and three-input NAND gates. (A one-input NAND is an inverter.)

Inputs				Outputs		
$E1$	$E2$	a	b	1	2	3
0	X	X	X	1	1	1
X	0	X	X	1	1	1
1	1	0	0	1	1	1
1	1	0	1	0	1	1
1	1	1	0	1	0	1
1	1	1	1	1	1	0

11. Design, using AND, OR, and NOT gates, a priority encoder with seven active low inputs, $1', \dots, 7'$ and three active high outputs, CBA that indicate which is the highest priority line active. Input $1'$ is highest priority; $7'$ is lowest. If none of the inputs are active, the output is 000. There is a fourth output line, M , which is 1 if there are multiple active inputs.
- ★ 12. Implement the function
- $$f(x, y, z) = \sum m(0, 1, 3, 4, 7)$$

using two-way multiplexers.

13. In the following circuit, the decoder (DCD) has two inputs and four (active high) outputs (such that, for example, output 0 is 1 if and only if inputs A and B are both 0). The three multiplexers each have two select inputs (shown on the top of the box), four data inputs (shown on the left) and an active high enable input (shown on the bottom). Inputs A, B, C , and D are select inputs; inputs N through Z are data inputs. Complete a truth giving the value of F for each of the 16 possible select input combinations. (Comment: For some values, $F = 0$; for one value, $F = W$.)